REMARKS

Claims 1-23 are currently pending in the subject application and are presently under consideration. Favorable reconsideration of the subject patent application is respectfully requested in view of the comments herein.

I. Rejection of Claims 1, 2, 4, 6, and 13 Under 35 U.S.C. §102(b)

Claims 1, 2, 4, 6, and 13 stand rejected under 35 U.S.C. §102(b) as being anticipated by Batchelder, *et al.* (U.S. 4,647,172). It is respectfully requested that this rejection be withdrawn for at least the following reasons. Batchelder, *et al.* does not teach or suggest each and every element as set forth in the claimed invention.

> A single prior art reference anticipates a patent claim only if it expressly or inherently ***describes each and every limitation*** set forth in the patent claim. *Trintec Industries, Inc., v. Top-U.S.A. Corp.*, 295 F.3d 1292, 63 U.S.P.Q.2D 1597 (Fed. Cir. 2002). "A claim is anticipated only if ***each and every element*** as set forth in the claim is found, either expressly or inherently ***described*** in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The ***identical invention*** must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

In particular, independent claim 1 recites a ***develop chamber*** with an ***image collector, located at least partially therein,*** that collects ***energy reflected*** from inside the develop chamber and ***transmits a signal indicative of interior of the chamber.*** Batchelder, *et al.* does not teach or suggest such aspects of the claimed invention. In the Final Office Action (dated August 12, 2004), it is asserted that Batchelder, *et al.* teaches the claimed invention, and the Examiner references claims 1 and 3 of Batchelder, *et al.* to support this assertion. However, these sections of Batchelder, *et al.* do not mention placing ***an image collector at least partially within a develop chamber***, collecting ***reflected energy*** within ***the develop chamber*** with the image collector, and ***transmitting a signal indicative of the interior of the develop chamber*** as recited in the subject claims. Rather, claims 1 and 3 of Batchelder, *et al.* recite spraying developer on the

wafer surface to cause development of the resist, sensing light scattered back from an illuminated spot on the wafer surface with a photodetector, generating a voltage signal from the scattered light, and comparing the voltage signal with a reference signal to determine when to terminate development. Thus, at most, Batchelder, *et al.* discloses sensing ***scattered light*** (not reflected energy) and generating ***a signal for a spot on the surface of a wafer*** (not a signal indicative of the interior of a develop chamber), and Batchelder, *et al.* is silent regarding a develop chamber and positioning an image collector at least partially therein. Claims 1 and 3 of Batchelder, *et al.* are reproduced below.

> 1. Apparatus for developing exposed resist on the surface of a semiconductor wafer during fabrication of integrated circuits which comprises:
>
> means for spinning the wafer;
>
> means for spraying developer on the wafer surface to cause development of the resist;
>
> means illuminating at least a spot on the wafer surface from an incandescent light source;
>
> a photodetector, for sensing light scattered back from the illuminated spot on the wafer surface and generating therefrom a signal voltage;
>
> means for periodically digiting said voltage to generate sample data;
>
> means for storing reference data representing a template characteristic of a representative development process, said reference data including a reference control point which characterizes a known point in the reference development process;
>
> means for comparing the sample data and the reference data to obtain a best fit and to thereby locate a control point in the sample data which corresponds to the reference control point; and
>
> means for terminating development a calculated time interval after said sample control point.

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> 3. Apparatus for developing exposed resist on the surface of a semiconductor wafer during fabrication of integrated circuits which comprises:
>
> means for spinning the wafer;
>
> means for spraying developer on the wafer surface to cause development of the resist;
>
> means illuminating at least a spot on the wafer surface during development from an incandescent light source filtered to provide only non-exposing wavelengths;
>
> a photodetector, for sensing light scattered back from the illuminated spot on the wafer surface and generating therefrom a signal voltage;
>
> means for periodically digiting said voltage to generate sample data;
>
> means for storing reference data representing a template characteristic of optical fringes generated by a representative development process, said reference data including a reference control point which means for analyzing the sample data to locate a control point in the sample data which characterizes a last fringe in the reference development process; and
>
> means for terminating development a calculated time interval after said control point.

Since Batchelder, *et al.* does not teach or suggest each and every element as set forth in the claimed invention, the reference does not anticipate the subject claims. Accordingly, this rejection should be withdrawn.

II. Rejection of Claims 1-3, 5-7, 10-12, and 15-23 Under 35 U.S.C. §103(a)

Claims 1-3, 5-7, 10-12, and 15-23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Sanada (U.S. 5,843,527) in view of Ogata (U.S. 6,313,903). It is respectfully requested that this rejection be withdrawn for at least the following reasons. There is no suggestion or motivation in either reference to modify Sanada in view of Ogata or to combine the references to teach the subject claims.

> To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness. A *prima facie* case of obviousness is established by a showing of three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the

> knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

Independent claims 1, 15 and 19 recite a ***develop chamber*** with an ***image collector located at least partially therein***, wherein the image collector collects energy reflected from inside the develop chamber and transmits a signal indicative of interior of the chamber. In the Final Office Action, it is conceded that "Sanada does not teach the chamber is a developer." However, the Examiner then asserts that Ogata teaches a coater and developer unit and that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the references to teach the claimed invention because the coater and developer are the same unit. Applicants' representative respectfully disagrees. In particular, Ogata teaches a fabrication system that includes a wafer inspecting unit 15, which is separated from the coater and developer unit 13 by an interface 14. (*See* col. 1, lines 38-41). As disclosed in Ogata, after a wafer is coated and developed it is transferred to this inspecting unit, which is utilized to inspect line width, overlap, coating irregularities, and developing defect. (*See* col. 1, lines 38-44). If the wafer is deemed acceptable, it is transferred to the next process, and if the wafer is deemed unacceptable it is washed and re-submitted to the coater and developer unit. (*See* col. 1, lines 45-59). However, Ogata is silent regarding monitoring either a coating or developing process, or collecting reflected energy within a develop chamber.

It is respectfully submitted that simply because the coater and developer of Ogata are one unit does not mean it would be obvious to combine the teachings of Sanada and Ogata to render applicants' claimed invention. Rather, "[a] teaching or suggestion to make the claimed combination and a reasonable expectation of success must both be found in the prior art...." (*See In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)) and "the mere fact that references can be modified does not render the modification obvious unless the cited art also suggests the desirability of the modification" (*In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)). Since Sanada relates to visually monitoring of a coating process and Ogata teaches a wafer

inspection unit separate from a coating and developing process, applicants' representative submits that there is no teaching, suggestion, motivation or desirability (it would not have been obvious) to combine these references; it would not be obvious at the time of the invention to one of ordinary skill who was monitoring a coating process to look to a reference that does not teach or suggest monitoring a coating process or a development process, but instead teaches a post coating and development wafer inspection.

Thus, neither Sanada nor Ogata provide any teaching, suggestion, motivation or desirability to be modified in view of the other or to be combined to result in applicants' claimed invention. Therefore, this rejection should be withdrawn

CONCLUSION

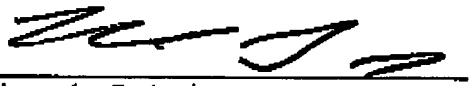
The present application is believed to be in condition for allowance in view of the above comments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063.

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

AMIN & TUROCY, LLP



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